We claim:

1. A method for distributing a clock signal generated by a clock generator to a plurality of nodes on an integrated circuit, said method comprising the steps of:

estimating the clock delay for each of said nodes, wherein said clock delay includes clock generator output delays and resistive-capacitive (RC) delays; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase.

2. The method of claim 1, wherein said estimating step further comprises the step of estimating a round trip delay time for said clock signals.

3. The method of claim 2, wherein said round trip delay time is obtained using a primary clock path and a return clock path.

4. The method of claim 1, wherein said integrated circuit is a system-on-chip (SoC).

5. The method of claim 1, wherein said integrated circuit is a printed circuit board (PCB).

6. A method for distributing a clock signal generated by a clock generator to a plurality of nodes on an integrated circuit, said method comprising the steps of:

providing a feedback clock path for each of said nodes, each of said feedback clock paths having an associated primary clock path that distributes said clock to each node;

determining a round trip travel time of said clock signal on each of said primary clock paths and associated feedback clock path;

estimating the clock delay for each of said nodes using said round trip travel time; and

adjusting said clock signal for each node based on said estimated clock delay such that said clock signal arrives at each of said nodes with an aligned phase.

7. The method of claim 6, wherein said clock delay includes a clock generator output delay and a resistive-capacitive (RC) delay.

8. The method of claim 6, wherein said estimating step further comprises the step of estimating a round trip delay time for said clock signals.

9. The method of claim 8, wherein said round trip delay time is obtained using a primary clock path and a return clock path.

10. The method of claim 6, wherein said integrated circuit is a system-on-chip (SoC).

11. The method of claim 6, wherein said integrated circuit is a printed circuit board (PCB).

12. A network for distributing a clock signal generated by a clock generator to a plurality of nodes on an integrated circuit, said network comprising:

a primary clock path that distributes said clock to each node;

a feedback clock path associated with each of said primary clock paths;

a phase comparator for determining a round trip travel time of said clock signal on each of said primary clock paths and associated feedback clock path; and

a delay driver for adjusting said clock signal for each of said nodes based on an estimated clock delay for each of said nodes based on said round trip travel time, such that said clock signal arrives at each of said nodes with an aligned phase.

13. The network of claim 12, wherein said clock delay includes a clock generator output delay and a resistive-capacitive (RC) delay.

14. The network of claim 12, wherein said estimating step further comprises the step of estimating a round trip delay time for said clock signals.

15. The network of claim 14, wherein said round trip delay time is obtained using a primary clock path and a return clock path.

16. The network of claim 12, wherein said integrated circuit is a system-on-chip (SoC).

17. The network of claim 12, wherein said integrated circuit is a printed circuit board (PCB).